CMOS Bandgap Reference and Current Reference with Simplified Start-Up Circuit

Guo-Ming SUNG, Ying-Tzu LAI, Chien-Lin LU
Department of Electrical Engineering, National Taipei University of Technology
1, Sec. 3, Chung-Hsiao E. Rd. Taipei 10608 Taiwan
1gmsung@ntut.edu.tw; 2t5319013@ntut.edu.tw; 3lu8169@yahoo.com.tw

Abstract

This paper presents a CMOS bandgap reference and current reference based on the resistor compensation. The proposed architecture consists of various high positive temperature coefficient (TC) resistors, a two-stage operational transconductance amplifier (OTA) and a simplified start-up circuit in 0.35-µm CMOS process. In the proposed bandgap reference and current reference, numerous compensated resistors, which have a high positive temperature coefficient (TC), are added to the parasitic n-p-n and p-n-p bipolar junction transistor devices, to generate a temperature-independent voltage reference and current reference. With the simplified start-up circuit, the proposed resistor-compensation bandgap reference and current reference can be started at 43 ns at a minimum supply voltage of 1.35 V. The measurements verify the current reference of 735.6 nA, the voltage reference of 888.1 mV, and the power consumption of 91.28 µW at a supply voltage of 3.3 V. The voltage TC is 49 ppm/℃ in the temperature range from 0℃ to 100℃ and 12.8 ppm/℃ from 30℃ to 100℃. The current TC is 119.2 ppm/℃ at temperatures of 0℃ to 100℃. Measurement results also demonstrate a stable voltage reference at high temperature (> 30℃), and a constant current reference at low temperature (< 70℃).

Keywords
Bandgap Reference; Current Reference; Resistor Compensation; Temperature Coefficient; Start-up Circuit

Introduction

A bandgap reference is extensively adopted in several integrated circuits, including analog, mixed-mode and memory circuits. In CMOS bandgap reference design, the sub-1-V curvature-compensated CMOS bandgap reference is favored for use with resistive subdivision methods [1-3], parasitic n-p-n and p-n-p bipolar junction transistor devices [4], and the compensation approaches associated with layout, operational amplifiers, and VBE linearization [5-7]. However, the low-voltage bandgap reference frequently functions with a higher temperature coefficient than the conventional bandgap reference [4]. To reduce the temperature coefficient further, many curvature compensations have been introduced. Guan et al. developed a current mode curvature-compensated BGR (bandgap reference) using the trimming approach [8]. Leung et al. introduced second-order curvature compensation based on resistors with opposing temperature coefficients [9]. Audy introduced a third-order curvature compensation with a low-TCR resistor in parallel with a high-TCR resistor and in series with low-TCR tail resistors [10]. Malcovati had designed a high-order curvature temperature compensation method with Malcovati topology [7]. Chen also presented a programmable and high-precision temperature independent current reference by adding a positive TC current to a negative TC circuit [11]. However, the simulation result had not been verified yet.

Start-up circuits are required to prevent the bandgap reference from operating at the zero point. The components of a start-up circuit must be limited to three or less. Xing et al. developed a start-up circuit that comprised three NMOSs, MS1-MS3 [5]. Xiaokang Guan et al. also introduced a start-up circuit with a resistor R6 and two PMOSs, M7-M8 [8]. Ker further developed two start-up circuits in the proposed bandgap reference. One consists of one PMOS and two NMOSs, MSD-MSP [4]. The other comprises a NMOS and two PMOSs, MSP1-MSP3 [4]. Unfortunately, as is well known, the rise times of the proposed start-up circuits are long. More effort must be made to design a high-speed start-up circuit. Additionally, the current trend in industry is toward new bandgap references with simultaneous voltage reference and current reference [3], [12]. If a temperature-independent current reference is required, then the bandgap reference must generally be divided by a resistance. However, the resistance depends on temperature. Accordingly, a current reference also depends on a curvature-compensation method. This work presents a resistor-
compensation CMOS bandgap and current reference with a current reference of 735.6 nA and a voltage reference of 888.1 mV at a supply voltage of 3.3 V in a standard 0.35-µm CMOS process. The proposed bandgap and current reference, which comprises a two-stage operational transconductance amplifier (OTA) with differential NMOS input stage, is validated. Notably, the voltage TC is 49 ppm/℃ in the temperature range from 0°C to 100°C, and 12.8 ppm/℃ from 30°C to 100°C; the power consumption is 91.28 µW. Hence, section II describes the basic principles and circuit designs associated with the proposed bandgap and current reference. Section III presents and discusses experimental results. Conclusions are finally drawn in Section IV, along with recommendations for future research.

**Basic Principles and Circuit Design**

**Basic Principles of CMOS Bandgap Reference**

The temperature-independent bandgap reference is the conventionally adopted voltage reference because temperature commonly skews the operating point and affects noise in the semiconductor. A bandgap reference working with zero TC, which has both positive TC and negative TC, is therefore required. Figure 1 depicts the basic framework of a bandgap reference [13-15]. The output reference voltage, \( V_{\text{ref}} \), is

\[
V_{\text{ref}} = V_{\text{EB}} + K \cdot V_t
\]

where \( K \) is a constant which is normally equal to 17.2 [13], \( V_{\text{EB}} \) is the voltage difference between the emitter and the base in bipolar junction transistors (BJT) and \( V_t \) is the thermal voltage. \( V_{\text{EB}} \) typically exhibits a negative-TC characteristic, while thermal voltage \( V_t \) usually has a positive TC. \( V_t \) is realized from the difference between two emitter-base voltages, \( \Delta V_{\text{EB}} \), which is proportional to the absolute temperature (PTAT). However, the output voltage of the bandgap reference suffers from variation with temperature, even when curvature-compensation is considered. To solve this problem, an improved cascading CMOS bandgap reference (BGR) with second-order curvature-compensated circuit has been presented [16]. However, it does not plot a temperature-independent current reference \( I_{\text{ref}} \). To have both voltage reference and current reference in a temperature-independent bandgap reference, the curvature-compensated method must be further investigated.

**Proposed Resistor Compensation Circuit**

Figure 2 presents the schematic of the proposed temperature-independent bandgap reference and current reference where a two-stage operational transconductance amplifier (OTA) is used to replace a traditional cascade current mirror. Notably, Resistors, \( R_3 \) and \( R_0 \), and BJT, \( Q_3 \), compensate for the output voltage reference, \( V_{\text{ref}} \), in what is called second-order curvature compensation [9]. Resistors \( R_0 \) and \( R_2 \) have two purposes. The first is to increase the input voltages, \( V_{\text{in+}} \) and \( V_{\text{in-}} \), of the N-type stage OTA to ensure that the OTA works properly. The second is to compensate for the temperature-dependent variation of \( V_{\text{in+}} \) and \( V_{\text{in-}} \). The OTA is employed to equality \( V_{\text{in+}} \) and \( V_{\text{in-}} \). Transistors \( Q_2 \) and \( Q_1 \) are vertical PNP's with a base-emitter area ratio of 5:2, passing the same current, such that the current through \( R_2 \) is PTAT. Transistors \( Q_1 \) and \( Q_3 \) are identical. \( R_b1, R_b2 \) and \( R_b3 \) are added to produce the second-order curvature compensation circuit [16]. Notably, the base-emitter area ratio of \( Q_2 \) and \( Q_1 \) is smaller than the traditional ratio, because current compensation is performed using several resistors. Therefore, the positive TCs of \( R_b1, R_b2 \) and \( R_b3 \) compensate for the negative temperature coefficients of \( Q_3, Q_2 \) and \( Q_1 \), respectively. MOSFETs \( M1-M4 \) are also identical to each other. They equalize the currents \( I_1, I_2, I_3 \) and \( I_{\text{ref}} \), and provide a temperature-independent current reference \( I_{\text{ref}} \). Restated, the proposed bandgap and current reference simultaneously provides both a temperature-independent voltage reference \( V_{\text{ref}} \) and temperature-independent current reference \( I_{\text{ref}} \).

Next, the resistor-compensation circuit is described in detail. The emitter-base voltage \( V_{\text{EB}} \) of BJT has a negative TC whereas the emitter-base voltage difference \( \Delta V_{\text{EB}} \) and all resistances have a positive TC.
As the temperature \( T \) increases, the voltages \( V_C, V_D \) and \( V_E \) of nodes C, D and E, will drop because of the negative TC of \( V_{EB} \); meanwhile, the values of compensated resistors, \( R_{b1}, R_{b2} \) and \( R_{b3} \), are increased. Three compensated currents flow into the three BJTs, \( Q_1, Q_2, \) and \( Q_3 \), respectively, compensating for the emitter currents, which increase according to a positive TC such that \( I_{R2} = (V_{EB1} - V_{EB2})/R_2 = \Delta V_{EB}/R_2 \). This increase yields three temperature-independent currents, \( I_1, I_2 \) and \( I_3 \). Simultaneously, voltages \( V_{in-}, V_{in+} \) and \( V_{ref} \) will be compensated for to maintain constant with resistances, \( R_{a1}, R_{a2} \) and \( R_3 \), because their TCs are positive. Hence, both voltage reference and current reference will be independent of temperature. We here need to emphasize that the compensated resistances, \( R_{b1}, R_{b2} \) and \( R_{b3} \), must be very large and be fabricated with n-wells. However, the resistance \( R_2 \), which is fabricated with n-diffusion, is low and a TC of around one-third of that of n-well. Figure 3 presents the five-corner simulations of current reference \( I_{ref} \) as a function of temperature for the proposed bandgap and current reference.

The proposed resistor-compensation circuit is analyzed mathematically. For simplicity, consider components \( R_{a2}, R_{a3}, R_3 \) and \( Q_3 \) in Fig. 2. Suppose that OTA is ideal and that the counterpart resistors are equal, such that \( V_{in} = V_{in+} \). Therefore, \( R_{a1} = R_{a2} \) and \( R_{b} = R_{b2} \); now, \( I_1 = I_2 \). Therefore,

\[
V_{EB1} + V_{Ra1} = V_{EB2} + V_{Ra2} + V_{R2} \tag{2}
\]

\[
V_{Ra1} = V_{Ra2} = I_{Ra1} \times R_{a1} = I_{Ra2} \times R_{a2} \tag{3}
\]

\[
I_{Ra2} = I_{Ra1} + I_{R2} = I_{Ra1} + I_{R2} \tag{4}
\]

Differentiating Eqn. (4) with respect to temperature \( T \) yields

\[
\frac{\partial I_{Ra2}}{\partial T} = \frac{\partial I_{R2}}{\partial T} + \frac{\partial I_{Ra2}}{\partial T} \tag{5}
\]

If a temperature-independent current reference \( I_{ref} \) is required, \( \partial I_{Ra2}/\partial T = 0 \) is set; thus,

\[
\frac{\partial I_{R2}}{\partial T} + \frac{\partial I_{R2}}{\partial T} = 0 \tag{6}
\]

where \( I_{Ra2} \) is a negative-TC current because \( I_{Ra2} = I_{Ra1} = V_{EB}/R_{a2} \), whereas \( I_{Ra1} \) is a positive-TC current because \( I_{Ra1} = (V_{EB1} - V_{EB2})/R_2 = \Delta V_{EB}/R_2 \). Combining the first differential item, \( \partial I_{Ra2}/\partial T \) with the second differential item, \( \partial I_{Ra2}/\partial T \), yields a temperature-independent current \( I_{R2} \). Passing through the current mirror, which has MOSFETs M1-M4, a temperature-independent current reference \( I_{ref} \) is generated in the proposed bandgap and current reference.

The voltage reference \( V_{ref} \) associated with the bandgap and current reference can be expressed as,

\[
V_{ref} = I_{R3} \times R_3 + V_{EB3} \tag{7}
\]

where \( V_{EB3} \) is the emitter to base voltage of the BJT Q3 and \( I_{R3} \) is the current through resistor \( R_3 \). Notably, \( I_{R3} \) equals \( I_3 \), which is a temperature-independent current. Differentiating the above equation with respect to temperature \( T \) yields

\[
\frac{\partial V_{ref}}{\partial T} = R_3 \times \frac{\partial I_{R3}}{\partial T} + I_{R3} \times \frac{\partial R_3}{\partial T} + \frac{\partial V_{EB3}}{\partial T} \tag{8}
\]
A temperature-independent bandgap reference is obtained by setting \( \frac{\partial V_{ref}}{\partial T} \approx 0 \) and \( \frac{\partial m}{\partial T} \approx 0 \). Therefore,

\[
I_{R3} \times \frac{\partial R_3}{\partial T} + \frac{\partial V_{EB3}}{\partial T} = 0
\]

(9)

where \( R_3 \) is a positive-TC resistor, whereas \( V_{EB3} \) is a negative-TC voltage. Properly setting the value of \( R_3 \) yields a temperature-independent voltage reference, \( \frac{\partial V_{ref}}{\partial T} \approx 0 \). Notably, \( R_3 \) not only compensates for the temperature variation of \( V_{EB3} \), but also adjusts the output voltage as required. Moreover, resistors \( R_3 \) and \( R_{R3} \) are fabricated using an n-well. The resistance \( R_3 \) exceeds \( R_{R3} \), while \( R_{R3} \) is less than \( R_{R4} \).

Figure 4 schematically depicts the complete circuit of the proposed bandgap and current reference, which simultaneously provides temperature-independent voltage reference \( V_{ref} \) and current reference \( I_{ref} \). The left-hand side of Fig. 4 presents an OTA circuit with N-type input [14], which is used to ensure that the positive input \( V_{in}^+ \) equals the negative input \( V_{in}^- \) of OTA. Notably, the MOSFET, \( M_t \), must be operated in the triode region as a resistor. The simulations of the two-stage telescopic OTA indicate that the dc gain, bandwidth and phase margins are 61.35 dB, 9.52 MHz and 64\(^\circ\), respectively. If an input offset voltage of OTA, owing to asymmetries, is considered, it will introduce error in the voltage reference \( V_{ref} \). Thus,

\[
V_{ref} = V_{EB3} + \left( \frac{R_3}{R_4} \right) \left( V_T \times \ln m - V_{OS} \right) + I_{R4} R_3
\]

(10)

where \( V_{OS} \) is the input offset voltage of OTA, \( V_T \) is the thermal voltage, and \( m \) is the base-emitter area ratio of Q2 to Q1, producing \( m \approx 5/2 \). In this work, two methods are employed to lower the effect of \( V_{OS} \). One is that the OTA is a telescopic topology to minimize the offset because of symmetry and the other is that the layout of OTA incorporates common centroid and dummy in a large device.

**Proposed Start-up Circuit**

As shown in Fig. 2, the start-up circuit comprises three MOSFETs, \( M_b, M_p \) and \( M_s \), where the gate-source voltage \( V_{CS} \) of \( M_b \) is shorted to turn off \( M_b \) with a huge resistance. Restated, the gate voltage of \( M_b, V_{MSG} \), is half of the supply voltage \( V_{DD} \) in the initial stage because both \( M_p \) and \( M_s \) are cut-off. As the supply voltage \( V_{DD} \) increases slowly, \( V_{OTA,in} \), which is connected to the gate terminal of \( M_p \), traces \( V_{DD} \) because the OTA is off and the voltage difference between source \( (V_{DD}) \) and gate of \( M_b \) is about zero due to the C\(_{OP} \) of \( M_p, M_1 \) and \( M_2 \). When \( M_s \) is turned on under the condition \( V_{DD} - V_{MSG} \geq |V_{thp}| \) with a threshold voltage of PMOS, \( |V_{thp}| \), a small conduction current \( I_{MS} \) flows. Then the conduction resistance between drain and source, \( R_{DS} \), of \( M_b \) is reduced. By comparing with the huge resistance of \( M_b \), the gate voltage of \( M_b \) increases. \( M_b \) flows current until \( V_{DD} \) is reduced to nearly 0 V. The voltage of \( V_{MSG} \) keeps \( V_{DD} \) due to parasitic capacitance.

Finally, the operation mode of \( M_p \) is changed from saturation to the linear region and \( M_b \) will be turned off. Note that the \( M_b \) is used not only to speed-up the rise time, but also to save power without driving current. Figure 5 plots the simulated results concerning the start-up circuit over time, where the symbols \( \Delta, m, * \) and \( \bullet \) represent the power-supply voltage \( (V_{DD}) \), the gate voltage of \( M_1 (V_{MSG}) \), the output voltage of OTA \( (V_{OTA,out}) \) and the source current of \( M_b (I_{MS}) \), respectively. Importantly, the minimum power supply, \( V_{DD,min} \), is approximately 1.35 V, and the difference between the power-supply voltage \( (V_{DD}) \) and the gate voltage of \( M_b (V_{MSG}) \), \( V_{DD} - V_{MSG} \), exceeds 0.7 V; the start time is around 43 ns, and the source current of \( M_b \), \( I_{MS} \), falls to zero.

**Experimental Results**

The proposed bandgap and current reference was fabricated with 0.35-\( \mu m \) 2P4M CMOS process. The layout is carefully considered to minimize the mismatches of the resistor and that of the transistor. Additionally, resistors \( R_{a1} \) and \( R_{a2} \) are implemented using n-well because of its large temperature coefficient, while n+-diffusion occurs in resistor \( R_2 \) with a small temperature coefficient. The temperature-dependent performance was measured over operating temperatures from 0°C to 100°C. Figures 6 and 7 plot the measured voltage reference \( V_{ref} \) and current reference \( I_{ref} \), respectively, of the proposed bandgap and current reference against temperature. Figure 6 indicates that the measured voltage reference is proportional to the temperature in the range 0°C to 30°C, and is roughly constant from 30°C to 100°C. The temperature coefficient of the voltage reference is approximately 49 ppm/°C and the maximum variation of \( V_{ref} \) is approximately 4.35 mV at a supply voltage of 3.3 V and temperatures from 0°C to 100°C. The corresponding values are 12.8 ppm/°C and 0.8 mV from 30°C to 100°C. Figure 7 reveals that the measured current reference is almost constant from 0°C to 70°C, but increases rapidly in
FIG. 4 COMPLETE CIRCUIT OF THE PROPOSED BANDGAP AND CURRENT REFERENCE WHICH SIMULTANEOUSLY PROVIDES TEMPERATURE-INDEPENDENT VOLTAGE REFERENCE AND CURRENT REFERENCE

The temperature coefficient of the current reference is about 119.3 ppm/°C and the maximum variation of $I_{ref}$ is about 8.77 nA at temperatures from 0°C to 100°C. Additionally, the variations in voltage reference are measured, and plotted in Fig. 8 versus the power supply voltage from 0 V to 3.6 V. The measurements also demonstrate that output voltages from 0.871 V to 0.888 V are roughly proportional to the power supplied from 1.4 V to 3.4 V. Notably, the proposed bandgap and current reference can be started up at a supply voltage of 1.35 V, and so is suitable for operating with battery cell.

Table I presents the measurements of the proposed bandgap and current reference. Table II compares the proposed resistor-compensation bandgap and current reference presented herein with other prior-art curvature-compensation bandgap references. In table II, the best voltage TC of 12.8 ppm/°C is superior to that of other bandgap references, except [5], and the best current TC of 119.2 ppm/°C is acceptable by comparing with reference [19]. Based on the comparison, the proposed bandgap and current reference is suitable for use at temperatures of over 30°C. However, the averaged current reference is lower. Note that large compensated resistors, $R_{b1}$, $R_{b2}$ and $R_{b3}$ were selected herein to reduce power consumption of

FIG. 5 SIMULATED RESULTS CONCERNING START-UP CIRCUIT OVER TIME IN NS. (A) VARIATIONS OF $V_{DD}$ (△), $V_{SS}$ (●) AND $V_{OUT}$ (★) IN VOLT (V). (B) SOURCE CURRENT OF MS (◆) IN MICRO AMPERES (µA)
the chip and high positive-TC resistors, \( R_{a1} \) and \( R_{a2} \), were adopted to compensate for the temperature-dependent variation of \( V_{in+} \) and \( V_{in} \) in OTA. Figure 9 presents a die microphotograph of the proposed bandgap and current reference fabricated in a 0.35-\( \mu \)m CMOS process. In this chip, two capacitors, \( C_1 \) and \( C_2 \), are connected to power supply and voltage reference, respectively, to alleviate the unstableness.

![Figure 9](image)

**FIG. 9** DIE MICROPHOTOGRAPH OF THE PROPOSED BANDGAP REFERENCE AND CURRENT REFERENCE FABRICATED IN A 0.35-\( \mu \)M CMOS PROCESS

**TABLE 1** MEASUREMENTS OF PROPOSED BANDGAP REFERENCE AND CURRENT REFERENCE

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Measurements</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical power supply (V)</td>
<td>3.3</td>
</tr>
<tr>
<td>Minimum power supply (V)</td>
<td>1.35</td>
</tr>
<tr>
<td>Averaged voltage reference (mV) (0°C~100°C)</td>
<td>888.1</td>
</tr>
<tr>
<td>Maximum variation of voltage reference (mV) (0°C~100°C)</td>
<td>4.35</td>
</tr>
<tr>
<td>Voltage temperature coefficient (ppm/°C) (0°C~100°C)</td>
<td>49</td>
</tr>
<tr>
<td>Averaged voltage reference (mV) (30°C~100°C)</td>
<td>888.7</td>
</tr>
<tr>
<td>Maximum variation of voltage reference (mV) (30°C~100°C)</td>
<td>0.8</td>
</tr>
<tr>
<td>Voltage temperature coefficient (ppm/°C) (30°C~100°C)</td>
<td>12.8</td>
</tr>
<tr>
<td>Voltage reference settling time (V/µs)</td>
<td>38.1</td>
</tr>
<tr>
<td>Averaged current reference (nA) (0°C~100°C)</td>
<td>735.6</td>
</tr>
<tr>
<td>Maximum variation of current reference (nA) (0°C~100°C)</td>
<td>8.77</td>
</tr>
<tr>
<td>Current temperature coefficient (ppm/°C) (0°C~100°C)</td>
<td>119.2</td>
</tr>
<tr>
<td>Power dissipation (µW)</td>
<td>91.28</td>
</tr>
<tr>
<td>Chip area (µm( \times )µm)</td>
<td>237 × 256</td>
</tr>
</tbody>
</table>

**Conclusions**

A resistor-compensation CMOS bandgap reference and current reference with a current reference of 735.6 nA and a voltage reference of 888.1 mV at a supply voltage of 3.3 V was presented. It consumes a maximum power of 91.28 µW. The voltage TC was 49
TABLE 2 COMPARISON AMONG THE CURVATURE-COMPENSATED BANDGAP REFERENCES

<table>
<thead>
<tr>
<th></th>
<th>This work</th>
<th>[17]</th>
<th>[18]</th>
<th>[19]</th>
<th>[5]</th>
<th>[3]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.35 µm</td>
<td>0.35 µm</td>
<td>0.25 µm</td>
<td>0.18 µm</td>
<td>0.18 µm</td>
<td>0.13 µm</td>
</tr>
<tr>
<td>Typical $V_{\infty}$ (V)</td>
<td>3.3</td>
<td>3.3</td>
<td>NA</td>
<td>1.0</td>
<td>1.1</td>
<td>1.2</td>
</tr>
<tr>
<td>Minimum $V_{\infty}$ (V)</td>
<td>1.35</td>
<td>NA</td>
<td>0.85</td>
<td>NA</td>
<td>0.90</td>
<td>NA</td>
</tr>
<tr>
<td>Averaged voltage reference (0°C-100°C)</td>
<td>888.1 mV</td>
<td>1173.2 mV</td>
<td>238.2 mV</td>
<td>598.5 mV</td>
<td>657 mV</td>
<td>630 mV</td>
</tr>
<tr>
<td>Voltage TC (0°C-100°C)</td>
<td>49 ppm/°C</td>
<td>47 ppm/°C</td>
<td>58 ppm/°C</td>
<td>125 ppm/°C</td>
<td>10-40 ppm/°C</td>
<td>29 ppm/°C</td>
</tr>
<tr>
<td>Voltage TC (30°C-100°C)</td>
<td>12.8 ppm/°C</td>
<td>(trimming)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Averaged current reference (nA) (0°C-100°C)</td>
<td>735.6 nA</td>
<td>NA</td>
<td>NA</td>
<td>144 µA</td>
<td>NA</td>
<td>50.2 µA</td>
</tr>
<tr>
<td>Current TC (0°C-100°C)</td>
<td>119 ppm/°C</td>
<td>NA</td>
<td>NA</td>
<td>185 ppm/°C</td>
<td>NA</td>
<td>18 ppm/°C</td>
</tr>
<tr>
<td>Temperature Range</td>
<td>0-100°C</td>
<td>-75-75°C</td>
<td>-10-120°C</td>
<td>0-100°C</td>
<td>0-150°C</td>
<td>-10-100°C</td>
</tr>
</tbody>
</table>

ppm/°C at temperatures from 0°C to 100°C, and 12.8 ppm/°C from 30°C to 100°C. The current TC was 119.2 ppm/°C from 0°C to 100°C. The measurements also reveal that a good temperature-independent voltage reference $V_{ref}$ is realized at high temperature and a fine temperature-independent current reference $I_{ref}$ is performed at low temperature. With a simplified start-up circuit, the proposed bandgap and current reference was verified to be effective in a standard 0.35-µm CMOS process. Restated, the proposed resistor-compensation CMOS bandgap and current reference, which is compensated with various high positive TC resistors, simultaneously provides both a temperature-independent voltage reference $V_{ref}$ and temperature-independent current reference $I_{ref}$.

Furthermore, this work verifies that both n-well and n+-diffusion are suitable for developing a new resistor-compensation technique in bandgap reference or current reference. To further improve the performance of bandgap reference or current reference, the resistor-compensation technique can be utilized except high-order curvature compensation [5].

ACKNOWLEDGMENT

The authors would like to thank the National Science Council of the Republic of China, Taiwan, for financially supporting this research under Contract No. NSC 95-2221-E-027-138-MY3. The CIC is appreciated for fabricating the test chip and Ted Knoy is appreciated for his editorial assistance.

REFERENCES


Guo-Ming Sung received the B.S. and M.S. degrees in biomedical Engineering from the Chung-Yuan University in 1987 and 1989, respectively, and the PH.D. degree in electrical engineering from the National Taiwan University, Taipei, in 2001. In 1992, he joined the Division of Engineering and Applied Sciences, National Science Council, Taiwan, where he became an Associate Researcher in 1996. Since 2001, he has been with the Electrical Engineering Department, National Taipei University of Technology, where he is an Associate Professor. His research interests include magnetic sensors, integrated circuits and systems for analog and digital circuits, motor control ICs, and mixed-mode ICs for XDSL.

Ying-Tzu Lai received the M.S. degree in electrical engineering from Lunghwa University of Science and Technology, Taoyuan, Taiwan, R.O.C., in 2005, and now studying Ph.D. degrees in electrical engineering from National Taipei University of Technology since 2006. Her research interests include mixed-mode integrated circuit design, analog-to-digital converters, and switched-current delta-sigma modulator.

Chien-Lin Lu received the B.S. degree from the Department of Communications Engineering, Feng Chia University in 2004, and now studying M.S. degrees in Electronic Engineering from National Taipei University of Technology since 2008. He has been a member with the National Chip Implementation Center (CIC), Taiwan, R.O.C. His research interests include analog circuit design, RF circuit design, and analog to digital converter (ADC).