A new FinFET flip-flop operating in low source voltages

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Abstract: A flip-flop is one of the most widely used cells in digital circuits. This paper proposed a new FinFET flip-flop operating in low source voltages. The four flip-flops using different design styles, named as master-slave flip-flop based on transmission gate, brute-force master-slave flip-flop based on clocked CMOS, and the proposed new flip-flop are compared in terms of delay time, power consumption, and power delay product. All circuits are simulated with HSPICE at a PTM (Predictive Technology Model) 32nm FinFET technology. The results show that the proposed flip-flop obtains good performance on delay, power consumption, and power delay product. Especially in low source voltages, the proposed flip-flop achieves great improvement in power delay product, compared with the other ones.

Keywords: Flip-flop, low voltage operating, high speed, low-power design.

1. Introduction

As the feature size for manufacturing transistor continued to shrink, the mainstream technology has reached to 16 nm. However, the following general CMOS transistor is facing serious challenges of short channel effect, and thus resulting in increasing leakage power consumption [1, 2]. Looking for a new structure of the device instead of the ordinary CMOS devices is imperative. As a 3D FinFET device, it has been to prove that it takes over ordinary CMOS transistors and continued to Moore's Law. Intel, TSMC, Samsung, and other foundries have realized FinFET mass productions.

As three-dimensional device, the structure of FinFET is different from the ordinary CMOS device. As shown in Fig. 1, the channel is wrapped by gate electrodes, which enhance the strength of the gate control for the device channel, and thus inhibit the short channel effect of devices, but also inhibits the leak current of device. The FinFETs have two modes, names as common-gate (CG) and independent-gate (IG) structure. The two gate of the common-gate FinFETs are connected together, while the two gates of the independent-gate symmetric FinFET structures can be used independently.

With the popularity of smart phones, tablet computers and other portable electronic products, extending battery life has become a main task for IC design engineers. Therefore, low-power circuit designs increasingly attracted the attention of IC design engineers [3, 4, 5]. The power dissipation of the circuits consists of three parts, namely as dynamic power, static leakage power consumption, and short-circuit power. Among them the dynamic power and static leakage power constitute to the main parts. Reducing the supply voltage is the most common way to reduce power consumption, and it can not only reduce dynamic power consumption but also reduce static leakage power consumption, because the square relation between dynamic power consumption and the power source voltage, and a linear relationship between static power and the power source voltage [2]. However, reducing the supply voltage would increase the delay cost of a circuit. Because the circuit current flow is small in low source voltage, we should increase the driving ability of the circuit by increasing the size of the devices. Compared with the conventional CMOS, the FinFET has higher turn-on current, and thus it can provide better drive strength. Therefore, FinFET logic circuits operating in medium strong inversion regions have more favorable performance than near-threshold circuits because of larger turn-on currents.

A flip-flop is a kind of basic circuit units, which is one of the important components. For many circuits, the performance of the flip-flops will be able to determine that the circuit performance is good or bad. Therefore, the flip-flop has become one of the main research object of the researchers [6, 7, 8]. To design a fast and low power consumption flip-flop has become one of the circuit designer inevitable question [9, 10].

In this paper, the four flip-flops that based on the FinFET using different design styles, named as master-slave flip-flop based on transmission gate, brute-force master-slave flip-flop based on transmission gate, brute-force master-slave flip-flop based on clocked CMOS, and a new flip-flop are analyzed and compared in terms of delay time, energy consumption, and energy delay product. All circuits are simulated with HSPICE at a PTM (Predictive Technology Model) 32nm FinFET technology [11, 12].

2. FinFET devices operating in low source voltages

The FinFET is manufactured as three-dimensional structure with a thin silicon body, as shown in Fig. 1 [11]. The gate electrodes wrap tightly the thin silicon body, and its thickness is usually denoted by \( t_w \). As shown in Fig. 1, the FinFET is manufactured as a double-gate structure. Its two gates can either be shorted or independently controlled to form two independent gates. The independent dual gates of the FinFET devices can be achieved by etching away the gate electrode at the top of the FinFET channel [13, 14]. In this work, we only consider SG (Short-Gate) mode, and all circuits use SG FinFET devices. The effective gate width of a SG FinFET is \( 2nH_{fin} \) where \( n \) is the number of FinFET’s fins, and \( H_{fin} \) is its height. The wider FinFETs are only obtained by using multiple fins (\( n \) fins).

Figure. 1 The structure and symbol of FinFET devices.

The simulation results for the 32nm n-type FinFET and conventional bulk NMOS transistor are carried out, and its current-voltage characteristics are shown in Fig. 2. From Fig. 2, the FinFET transistor obtains higher turn-on current than the conventional bulk one, and thus fast operating speed.
As shown in Fig. 2, the FinFET transistors obtain larger sub-threshold slope than the conventional bulk MOS ones because of the strong gate control to the device channel. On the one hand, the FinFET device has the less leakage than the conventional bulk MOS ones. Compared with bulk MOSFET, the FinFET device operating on medium strong inversion regions have more favorable performance than conventional bulk MOS ones because of larger turn-on currents.

A good comprehensive compromise between operating speed and power dissipation is PDP (Power Delay Product). The total power consumption \( P_{\text{total}} \) in a logic gate is expressed as Eq. (1)

\[
P_{\text{total}} = P_{\text{dyn}} + P_{\text{leakage}} = fC_s V_D^2 + V_{DD} I_{\text{leakage}}
\]

where \( C_s \) is the load capacitance of a logic gate, \( V_{DD} \) is source voltage, \( f \) is operation frequency, and \( I_{\text{leakage}} \) is leakage current of the FinFET devices in a logic gate. From (1), \( P_{\text{total}} \) scales down quadratically with the supply voltage. As supply voltage scales down, \( P_{\text{leakage}} \) is reduced linearly.

Assuming that the performance of P-type and N-type FinFETs is symmetrical, when the source voltage is larger than the threshold voltage of the device, the delay of a FinFET gate is Eq. (2)

\[
t_d = K C_s V_{DD} \frac{V_{TH}}{V_{DD}}
\]

where \( K \) is a delay fitting parameter, \( V_{TH} \) is threshold voltage, and \( \alpha \) is velocity saturation parameter, respectively. \( \alpha \) is about 1.3 in our simulations.

![Current-voltage characteristics of the 32 nm n-type FinFET and conventional bulk NMOS transistors.](image_url)

PDP (Power Delay Product) can be written as Eq. (3)

\[
PDP = P \times t_d
\]

Plugging (1) and (2) into (3) gives the PDP (Power Delay Product) as Eq. (4)

\[
PDP = \frac{(fC_s V_D^2 + V_{DD} I_{\text{leakage}})KC_s V_D}{(V_{DD} - V_{TH})^\alpha}
\]

3. Flip-flops based on FinFETs

In the sequential circuits, a flip-flop is the one of the basic cells that most frequently used. The performance of the flip-flops is often determines the performance of the circuits. Therefore, designing a suitable flip-flop is crucial for circuit designers.

The master-slave flip-flop based on transmission gate (TG flip-flop) is the simplest and most commonly used triggers, as shown in Fig. 3. It consists of 22 transistors. When the \( CLK \) as low, the main latch samples input signal \( D \), and the slave latch hold its state, and thus keep the output \( Q \) to be stabilized. In the rising edge of \( CLK \), the setup time of the circuit is the sum of three phase inverter with a transmission gate and time delay. Maintain time is approximately equal to zero. The propagation delay is equal to the delay a transmission gate and an inverter.

The master-slave brute-force flip-flop based on transmission gate (BF TG flip-flop) is simplified version of TG flip-flop, as shown Fig. 4. This circuit greatly reduces the circuit area compared with Fig. 3. It is made up of 12 transistors. This flip-flop must properly set the size of the transistor in the latches. In general, the size of the inverter is at least as twice large as the feedback inverter to trigger its state. The large transistor size of the inverters can be at the expense of the area and power consumptions.
Master-slave brute-force flip-flop based on clocked CMOS (BF C$^2$MOS flip-flop) use clocked CMOS triggers, which made up of 20 transistor, as shown in Fig. 5. It belongs to the pseudo static triggers. It not only rely on charging and discharging the node capacitance of the circuit for storage, also introduced static inverter chain structure of the latch, so called as pseudo static memory. C$^2$MOS is a kind of circuit structure that is not sensitive to clock overlapping phenomenon. When CLK is low, the master latch is sampled and the slave latch is in the maintain state. When the CLK is in the rising edge, the master latches become hold state, while the value of the master latch is transmitted from the slave latch to the output $Q$.

A new flip-flop is proposed with dual-rail inputs and single-rail output, as shown in Fig. 6. The flip-flop is made up of 13 transistors. When the CLK is high, the main latch samples dual-rail inputs, while the slave latch maintain its state. When CLK is low, the master latch is in the holding state, and the value of the master latch is transmitted from the slave latch to the output $Q$. The advantage of the structure of this circuit is that the transmission time is short, and it is equivalent to a transmission gate. Thus, the circuit can be used in high speed operation. Because of less transistor counter, we can expect that the proposed flip-flop has low power dissipations.
4. Simulations and results

The four flip-flops using different design styles, named as master-slave flip-flop based on transmission gate, brute-force master-slave flip-flop based on transmission gate, brute-force master-slave flip-flop based on clocked CMOS, and the proposed new flip-flop are compared in terms of delay time, power consumption, and power delay product. All circuits are simulated with HSPICE at a PTM (Predictive Technology Model) 32nm FinFET technology. We have made a comprehensive comparison and analysis of four different triggers, such as the setup time.

The settling time is shown in Fig. 7. The proposed flip-flop has minimum settling time, because of the proposed flip-flop is just the delay time of an inverter.

The propagation delay of the four flip-flops is shown in Fig. 8. The propagation delay of the proposed flip-flop is minimal. The delay of the proposed flip-flop is merely the delay of a transmission gate, which is suitable for application in high speed circuits. In the standard source voltage (1 V), the propagation delay of the proposed flip-flop is about 1/6 propagation delay of the master-slave flip-flop based on transmission gate.

![Setup time of the four flip-flops](image.png)
The power consumption of the four flip-flops is compared in Fig. 9. The power consumption of the circuit is decreased with the decrease of the power supply voltage. The proposed circuit has the lowest power consumption, because the phase-locked loop of the proposed flip-flop is virtual connected, and the fewer number of transistors used in the proposed flip-flop. In the standard source voltage (1 V), the power consumption of the proposed flip-flop is about 1/2 power dissipation of the master-slave flip-flop based on transmission gate.

The PDP of the four different flip-flops is compared in Fig. 10. The PDP of the proposed flip-flop is smallest. The circuit with smaller PDP has a good comprehensive performance. In the standard source voltage (1 V), the PDP based on the proposed flip-flop is about 1/8 of the master-slave flip-flop based on transmission gate.
5. Conclusions

A flip-flop is one of the most widely used cells in digital circuits. In this paper, a new flip-flop has been proposed. The four flip-flops using different design styles, named as master-slave flip-flop based on transmission gate, brute-force master-slave flip-flop based on transmission gate, brute-force master-slave flip-flop based on clocked CMOS, and the new flip-flop are compared in terms of delay time, power consumption, and power delay product. The results show that the new proposed flip-flop obtains good performance on delay, power consumption, and power delay product. Especially in low source voltages, the proposed flip-flop achieves great improvement in power delay product, compared with the other ones.

6. Acknowledgement

This work was supported by the National Natural Science Foundation of China (No. 61671259 and No. 61271137).

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